

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-021935

(43)Date of publication of application : 21.01.2000

(51)Int.Cl.

H01L 21/60

(21)Application number : 10-198126

(71)Applicant : CASIO COMPUT CO LTD

(22)Date of filing : 30.06.1998

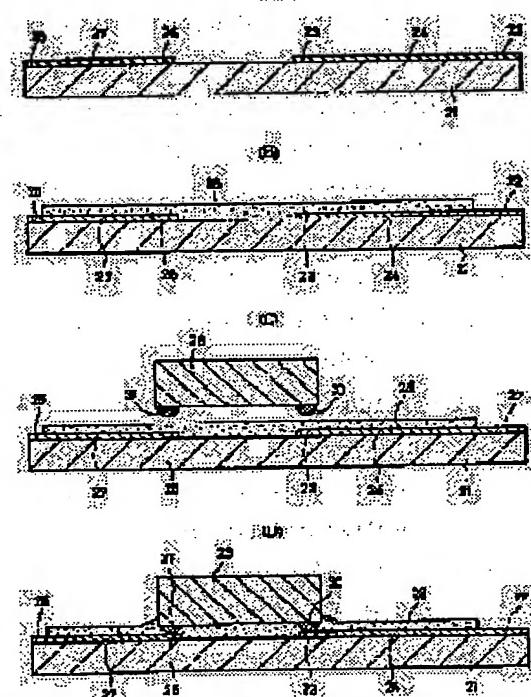
(72)Inventor : NOMURA TADAHIRO

## (54) ELECTRONIC COMPONENT MOUNTING BODY AND MANUFACTURE THEREOF

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To avoid degradation especially in sealing function with less number of manufacturing processes, in a mounting technology for semiconductor chips, comprising an LSI, etc., which is called COF(chip on film).

**SOLUTION:** On the upper surface of a film substrate 21, external connection pads 22 and 25, semiconductor chip connection pads 23 and 26, and routing wires 24 and 27 between them are formed. On the upper surface of the film substrate 21, a sealing/protective film 28 of a thermoplastic resin is formed at a part, except for the part of both external connection pads 22 and 25. Gold bumps 30 and 31 of a semiconductor chip 29 protrude into the sealing/protective film 28 for connection to the semiconductor chip connection pads 23 and 26. Here, the sealing/protective film 28 will not peel, even if the film substrate 21 is bent near the semiconductor chip 29, and moreover it is sufficient that only the sealing/protective film 28 be formed.



### LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

**BEST AVAILABLE COPY**

\* NOTICES \*

JPO and NCIPI are not responsible for any  
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

## CLAIMS

---

[Claim(s)]

[Claim 1] The electronic-parts mounting object characterized by to provide the wrap closure-cum-a protective coat for the part of the leading-about line of said film substrate while intervening between the film substrate with which the connection pad for electronic parts, the external connection pad, and the leading-about line in the meantime were formed in the field of 1, the electronic parts which were connected to this connection pad for electronic parts, and were carried in the part of the connection pad for electronic parts of said film substrate, and said electronic parts and said film substrate.

[Claim 2] It is the electronic-parts mounting object characterized by said the closure-cum-protective coat consisting of thermoplastics in invention according to claim 1.

[Claim 3] The manufacture approach of the electronic-parts mounting object which is on the field of 1 of the film substrate with which the connection pad for electronic parts, the external connection pad, and the leading-about line in the meantime were formed in the field of 1, and is characterized by to form the closure-cum-a protective coat in the part except the part of said external connection pad, to connect electronic parts to said connection pad for electronic parts, and to carry on the closure-cum-said protective coat in the part of the connection pad for electronic parts of said film substrate.

[Claim 4] It is the manufacture approach of the electronic-parts mounting object characterized by forming said the closure-cum-protective coat with thermoplastics in invention according to claim 3.

---

[Translation done.]

\* NOTICES \*

JPO and NCIPI are not responsible for any  
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

## DETAILED DESCRIPTION

---

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the electronic-parts mounting object which comes to

carry electronic parts on a film substrate, and its manufacture approach.

[0002]

[Description of the Prior Art] There is a technique called COF (Chip OnFilm) in the mounting technology of the semiconductor chip (electronic parts) which consists of LSI etc. Drawing 2 shows the sectional view of an example of the semiconductor chip mounting object (electronic-parts mounting object) manufactured by such conventional mounting technology. This semiconductor chip mounting object is equipped with the film substrate 1. The external connection pad 2 of an input side, the connection pad 3 for semiconductor chips, and the leading-about line 4 in the meantime are formed in the predetermined part of the top face of the film substrate 1, and the external connection pad 5 of an output side, the connection pad 6 for semiconductor chips, and the leading-about line 7 in the meantime are formed in other predetermined parts. On the top face of the film substrate 1, the protective coat 8 which consists of insulating ink for protecting the leading-about lines 4 and 7 is formed in the part except the part of both the external connection pads 2 and 5, and the part (that is, semiconductor chip loading field) of the connection pads 3 and 6 for both semiconductor chips. The semiconductor chip 9 which consists of LSI etc. is carried in the semiconductor chip loading field of the top face of the film substrate 1, where the bumps 10 and 11 prepared in the inferior surface of tongue are connected to the connection pads 3 and 6 for semiconductor chips. And when the ingredient of a sealing agent 12 is trickled into the perimeter of a semiconductor chip 9 by the dispenser, the sealing agent 12 for protecting the inferior surface of tongue of a semiconductor chip 9 (closure) is formed in the top face of the protective coat [ / between a semiconductor chip 9 and the film substrates 1 and near the semiconductor chip 9 ] 8.

[0003]

[Problem(s) to be Solved by the Invention] However, with such a conventional semiconductor chip mounting object, when the film substrate 1 was bent near the semiconductor chip 9, exfoliation arose in the interface of a sealing agent 12 and a protective coat 8, and there was a problem that the function of a sealing agent 12 might be spoiled. Moreover, since a protective coat 8 and a sealing agent 12 would be formed at a respectively different process, there was also a problem that the number of production processes increased. Especially the technical problem of this invention is a closure function's not being spoiled and lessening the number of production processes.

[0004]

[Means for Solving the Problem] The electronic-parts mounting object concerning invention according to claim 1 The film substrate with which the connection pad for electronic parts, the external connection pad, and the leading-about line in the meantime were formed in the field of 1, While intervening between the electronic parts which were connected to this connection pad for electronic parts, and were carried in the part of the connection pad for electronic parts of said film substrate, and said electronic parts and said film substrate, the wrap closure-cum-a protective coat is provided for the part of the leading-about line of said film substrate. The manufacture approach of the electronic-parts mounting object concerning invention according to claim 3 Are on the field of 1 of the film substrate with which the connection pad for electronic parts, the external connection pad, and the leading-about line in the meantime were formed in the field of 1, and the closure-cum-a protective coat is formed in the part except the part of said external connection pad. It is made to connect with said connection pad for electronic parts, and is made to carry electronic parts on said the closure-cum-protective coat in the part of the connection pad for electronic parts of said film substrate. Since what is necessary is according to this invention for an exfoliation phenomenon like before especially not to arise, therefore not to spoil a closure function, since the closure-cum-the protective coat is made to combine a closure function and a protection feature, and to form only the closure-cum-a protective coat, the number of

production processes can be lessened.

[0005]

[Embodiment of the Invention] Drawing 1 (A) – (D) shows each production process of the semiconductor chip mounting object in 1 operation gestalt of this invention, respectively. Then, with reference to these drawings, the structure and its manufacture approach of the semiconductor chip mounting object in this operation gestalt are explained to order.

[0006] First, by carrying out patterning of the electric conduction film which consists of copper foil laminated on the top face of the film substrate 21 which consists of polyimide, polyethylene terephthalate, etc., aluminium foil, etc., as shown in drawing 1 (A) While forming the external connection pad 22 of an input side, the connection pad 23 for semiconductor chips, and the leading-about line 24 in the meantime in the predetermined part of the top face of the film substrate 21 The external connection pad 25 of an output side, the connection pad 26 for semiconductor chips, and the leading-about line 27 in the meantime are formed in other predetermined parts. Next, deposits (not shown), such as gold, tin, and solder, are formed by electrolytic plating or electroless deposition on the external connection pads 22 and 25, the connection pads 23 and 26 for semiconductor chips and the leading-about line 24, and 27.

[0007] Next, as shown in drawing 1 (B), the closure-cum-the protective coat 28 of predetermined thickness is formed by applying the transparency or the translucent thermoplastics of a thermoplastic epoxy resin, B-stage epoxy resin, etc. to the part except the part of both the external connection pads 22 and 25 with print processes, a dispenser, etc. on the top face of the film substrate 21, or laminating a sheet-like thing. Next, heating of about 1 hour is performed with the resin temperature of about 150 degrees C, and the closure-cum-the protective coat 28 is stiffened to some extent. Next, as shown in drawing 1 (C), using the bonding head with an adsorption device which is not illustrated, alignment of the semiconductor chip 29 which consists of LSI which has the bumps 30 and 31 who become an inferior surface of tongue from gold etc. is carried out above the semiconductor chip loading field of the top face of the film substrate 21, and it is arranged to it. Alignment in this case is performed when the closure-cum-the protective coat 28 carries out an image check with transparency or the camera which does not illustrate the connection pads 23 and 26 for semiconductor chips under the closure-cum-this protective coat 28, since it is translucent.

[0008] Next, as shown in drawing 1 (D), a semiconductor chip 29 is dropped with a bonding head, and face down bonding is performed. Resin temperature makes the bonding conditions in this case as an example about 1 – 10 seconds above the melting point (about 200–250 degrees C). Then, it caves in into the closure-cum-the protective coat 28 to which the bumps 30 and 31 of a semiconductor chip 29 were heated more than the melting point, and became soft, and connects with the connection pads 23 and 26 for semiconductor chips. Moreover, the closure-cum-the protective coat 28 in the perimeter of a semiconductor chip 29 is rising a little, and will be in a wrap condition about the lower peripheral face of a semiconductor chip 29. And when the closure-cum-the protective coat 28 hardens, the inferior surface of tongue of a semiconductor chip 29 is especially pasted up on the film substrate 21 through the closure-cum-the protective coat 28 under it. In this way, a semiconductor chip 29 is carried in the semiconductor chip loading field of the top face of the film substrate 21.

[0009] thus, with the acquired semiconductor chip mounting object Since it will have the function to take about with the function in which the closure-cum-the protective coat 28 protects the inferior surface of tongue of a semiconductor chip 29 (closure), and to protect lines 24 and 27 Since what is necessary is for an exfoliation phenomenon like before especially not to arise, not to spoil a closure function, and to form only the closure-cum-the protective coat 28, even if the film substrate 21 is bent near the semiconductor chip 29, the number of production processes can be lessened.

[0010] Here, an example of the dimension of this semiconductor chip mounting object is explained. The thickness of wiring of the external connection pad 22 and 25 grades is about 8-18 micrometers. The thickness on the film substrate 21 of the closure-cum-the protective coat 28 is about 1.5 to 2 times of the height of the bumps 30 and 31 of a semiconductor chip 29. The thickness on wiring of the external connection pad 22 of the closure-cum-the protective coat 28 and 25 grades is almost the same as the height of the bumps 30 and 31 of a semiconductor chip 29. Therefore, if bumps' 30 and 31 height is about 15 micrometers, the thickness on wiring of the external connection pad 22 of the closure-cum-the protective coat 28 and 25 grades is also about 15 micrometers.

[0011] In addition, although the above-mentioned operation gestalt explained the case where the front face of the closure-cum-the protective coat 28 was made flat as shown in drawing 1 (C), it is not limited to this. For example, the front face of the closure-cum-the protective coat 28 in the part corresponding to the inferior-surface-of-tongue center section of the semiconductor chip 29 is heaped up suitably, and while the peak top concerned forces and carries out flattening of the section on the inferior surface of tongue of a semiconductor chip 29 at the time of bonding, you may make it extrude Ayr which exists between the inferior surface of tongue of a semiconductor chip 29, and the front face of the closure-cum-the protective coat 28. When it does in this way, the adhesion force between a semiconductor chip 29 and the closure-cum-the protective coat 28 can be raised.

[0012] Moreover, although the above-mentioned operation gestalt explained the case where patterning of the electric conduction film which consists of copper foil laminated on the top face of the film substrate 21 was carried out, it may be made to carry out patterning of the electric conduction film which consists of copper foil laminated through the adhesives layer on the top face of not only this but the film substrate 21. Furthermore, although the above-mentioned operation gestalt explained the case where bumps 30 and 31 were formed in a semiconductor chip 29, you may make it prepare a bump on the connection pad 24 for semiconductor chips of not only this but the film substrate 21, and 27. However, when the connection pad of a semiconductor chip 29 is formed of aluminum, in order to make ohmic contact good, a metal layer (for example, two-layer structure of a TiW layer and Au layer or two-layer structure of Ti layer and Au layer) is formed on the connection pad which consists of aluminum of a semiconductor chip 29.

#### [0013]

[Effect of the Invention] Since what is necessary is according to this invention for an exfoliation phenomenon like before especially not to arise, not to spoil a closure function, since the closure-cum-the protective coat is made to combine a closure function and a protection feature, and to form only the closure-cum-a protective coat, as explained above, the number of production processes can be lessened.

---

[Translation done.]

\* NOTICES \*

JPO and NCIP are not responsible for any  
damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

## DESCRIPTION OF DRAWINGS

---

[Brief Description of the Drawings]

[Drawing 1] (A) – (D) is the sectional view of each production process of a semiconductor chip mounting object [ in / respectively / 1 operation gestalt of this invention ].

[Drawing 2] The sectional view of an example of the conventional semiconductor chip mounting object.

[Description of Notations]

21 Film Substrate

22 25 External connection pad

23 26 Connection pad for semiconductor chips

24 27 Leading-about line

28 Closure-cum-Protective Coat

29 Semiconductor Chip

---

[Translation done.]

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開2000-21935

(P2000-21935A)

(43)公開日 平成12年1月21日(2000.1.21)

(51)Int.Cl.<sup>7</sup>

H 01 L 21/60

識別記号

3 1 1

F I

H 01 L 21/60

マーク(参考)

3 1 1 W 4 M 1 0 5

(21)出願番号 特願平10-198126  
(22)出願日 平成10年6月30日(1998.6.30)

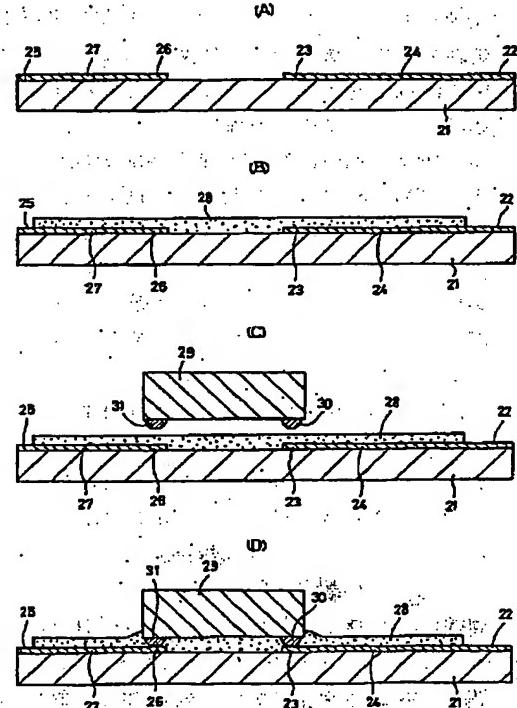
(71)出願人 000001443  
カシオ計算機株式会社  
東京都渋谷区本町1丁目6番2号  
(72)発明者 野村 直裕  
高知県南国市久礼田2420 高知カシオ株式  
会社内  
(74)代理人 100074985  
弁理士 杉村 次郎  
F ターム(参考) 4M105 AA03 BB11 CC16

(54)【発明の名称】電子部品実装体及びその製造方法

(57)【要約】

【課題】C O F (Chip On Film)と呼ばれるLSI等からなる半導体チップの実装技術において、特に封止機能が損なわれることがなく、また製造工程数を少なくする。

【解決手段】フィルム基板21の上面には外部接続パッド22、25、半導体チップ用接続パッド23、26及びその間の引き回し線24、27が形成されている。フィルム基板21の上面において両外部接続パッド22、25の部分を除く部分には熱可塑性樹脂からなる封止兼保護膜28が形成されている。半導体チップ29の金パンプ30、31は封止兼保護膜28中に減り込み、半導体チップ用接続パッド23、26に接続されている。この場合、フィルム基板21が半導体チップ29の近傍で折り曲げられても、封止兼保護膜28が剥離することがなく、また封止兼保護膜28のみを形成すればよい。



(2)

**【特許請求の範囲】**

**【請求項 1】** 一の面に電子部品用接続パッド、外部接続パッド及びその間の引き回し線が設けられたフィルム基板と、前記フィルム基板の電子部品用接続パッドの部分に該電子部品用接続パッドに接続されて搭載された電子部品と、前記電子部品と前記フィルム基板との間に介在されているとともに前記フィルム基板の引き回し線の部分を覆う封止兼保護膜とを具備することを特徴とする電子部品実装体。

**【請求項 2】** 請求項 1 記載の発明において、前記封止兼保護膜は熱可塑性樹脂からなっていることを特徴とする電子部品実装体。

**【請求項 3】** 一の面に電子部品用接続パッド、外部接続パッド及びその間の引き回し線が設けられたフィルム基板の一の面上であって前記外部接続パッドの部分を除く部分に封止兼保護膜を形成し、前記フィルム基板の電子部品用接続パッドの部分における前記封止兼保護膜上に電子部品を前記電子部品用接続パッドに接続させて搭載することを特徴とする電子部品実装体の製造方法。

**【請求項 4】** 請求項 3 記載の発明において、前記封止兼保護膜は熱可塑性樹脂によって形成することを特徴とする電子部品実装体の製造方法。

**【発明の詳細な説明】****【0001】**

**【発明の属する技術分野】** この発明は、フィルム基板上に電子部品を搭載してなる電子部品実装体及びその製造方法に関する。

**【0002】**

**【従来の技術】** L S I 等からなる半導体チップ（電子部品）の実装技術には、COF (Chip On Film) と呼ばれる技術がある。図 2 は従来のこのような実装技術によって製造された半導体チップ実装体（電子部品実装体）の一例の断面図を示したものである。この半導体チップ実装体はフィルム基板 1 を備えている。フィルム基板 1 の上面の所定の箇所には入力側の外部接続パッド 2、半導体チップ用接続パッド 3 及びその間の引き回し線 4 が設けられ、他の所定の箇所には出力側の外部接続パッド 5、半導体チップ用接続パッド 6 及びその間の引き回し線 7 が設けられている。フィルム基板 1 の上面において両外部接続パッド 2、5 の部分及び両半導体チップ用接続パッド 3、6 の部分（つまり半導体チップ搭載領域）を除く部分には、引き回し線 4、7 を保護するための絶縁性インクからなる保護膜 8 が設けられている。フィルム基板 1 の上面の半導体チップ搭載領域には L S I 等からなる半導体チップ 9 が、その下面に設けられたバンプ 10、11 を半導体チップ用接続パッド 3、6 に接続された状態で、搭載されている。そして、半導体チップ 9 の周囲に封止材 12 の材料がディスペンサによって滴下されることにより、半導体チップ 9 とフィルム基板 1 の間及び半導体チップ 9 の近傍における保護膜 8 の上面に

は、半導体チップ 9 の下面を保護（封止）するための封止材 12 が設けられている。

**【0003】**

**【発明が解決しようとする課題】** しかしながら、従来のこのような半導体チップ実装体では、フィルム基板 1 が半導体チップ 9 の近傍で折り曲げられた場合、封止材 12 と保護膜 8 との界面で剥離が生じ、封止材 12 の機能が損なわれてしまうことがあるという問題があった。また、保護膜 8 と封止材 12 とをそれぞれ別の工程で形成することになるので、製造工程数が多くなるという問題もあった。この発明の課題は、特に封止機能が損なわれる事なく、また製造工程数を少なくすることである。

**【0004】**

**【課題を解決するための手段】** 請求項 1 記載の発明に係る電子部品実装体は、一の面に電子部品用接続パッド、外部接続パッド及びその間の引き回し線が設けられたフィルム基板と、前記フィルム基板の電子部品用接続パッドの部分に該電子部品用接続パッドに接続されて搭載された電子部品と、前記電子部品と前記フィルム基板との間に介在されているとともに前記フィルム基板の引き回し線の部分を覆う封止兼保護膜とを具備したものである。請求項 3 記載の発明に係る電子部品実装体の製造方法は、一の面に電子部品用接続パッド、外部接続パッド及びその間の引き回し線が設けられたフィルム基板の一の面上であって前記外部接続パッドの部分を除く部分に封止兼保護膜を形成し、前記フィルム基板の電子部品用接続パッドの部分における前記封止兼保護膜上に電子部品を前記電子部品用接続パッドに接続させて搭載するようとしたものである。この発明によれば、封止兼保護膜に封止機能と保護機能とを兼ね備えさせているので、従来のような剥離現象が生じることなく、したがって特に封止機能が損なわれる事なく、また封止兼保護膜のみを形成すればよいので、製造工程数を少なくすることができます。

**【0005】**

**【発明の実施の形態】** 図 1 (A) ~ (D) はそれぞれこの発明の一実施形態における半導体チップ実装体の各製造工程を示したものである。そこで、これらの図を順に参照して、この実施形態における半導体チップ実装体の構造及びその製造方法について説明する。

**【0006】** まず、図 1 (A) に示すように、ポリイミドやポリエチレンテレフタレート等からなるフィルム基板 21 の上面にラミネートされた銅箔やアルミニウム箔等からなる導電膜をパターニングすることにより、フィルム基板 21 の上面の所定の箇所に入力側の外部接続パッド 22、半導体チップ用接続パッド 23 及びその間の引き回し線 24 を形成するとともに、他の所定の箇所に出力側の外部接続パッド 25、半導体チップ用接続パッド 26 及びその間の引き回し線 27 を形成する。次に、

(3)

3

外部接続パッド22、25、半導体チップ用接続パッド23、26及び引き回し線24、27上に電解メッキあるいは無電解メッキにより金、錫、半田等のメッキ層(図示せず)を形成する。

【0007】次に、図1(B)に示すように、フィルム基板21の上面において両外部接続パッド22、25の部分を除く部分に、熱可塑性エポキシ樹脂やBーステージエポキシ樹脂等の透明または半透明な熱可塑性樹脂を印刷法やディスペンサ法等により塗布したりシート状のものをラミネートしたりすることにより、所定の厚さの封止兼保護膜28を形成する。次に、樹脂温度150℃程度で1時間程度の加熱を行い、封止兼保護膜28をある程度硬化させる。次に、図1(C)に示すように、下面に金等からなるバンプ30、31を有するLSI等からなる半導体チップ29を、図示しない吸着機構付きポンディングヘッドを用いて、フィルム基板21の上面の半導体チップ搭載領域の上方に位置合わせして配置する。この場合の位置合わせは、封止兼保護膜28が透明または半透明であるので、この封止兼保護膜28下の半導体チップ用接続パッド23、26を図示しないカメラで画像確認すること等によって行われる。

【0008】次に、図1(D)に示すように、半導体チップ29をポンディングヘッドと共に下降させ、フェースダウンポンディングを行う。この場合のポンディング条件は、一例として、樹脂温度が融点以上(200~250℃程度)で1~10秒程度とする。すると、半導体チップ29のバンプ30、31が、融点以上に加熱されて軟らかくなつた封止兼保護膜28中に減り込み、半導体チップ用接続パッド23、26に接続される。また、半導体チップ29の周囲における封止兼保護膜28がやや盛り上がって、半導体チップ29の下部外周面を覆う状態となる。そして、封止兼保護膜28が硬化することにより、特に半導体チップ29の下面是その下の封止兼保護膜28を介してフィルム基板21上に接着される。かくして、フィルム基板21の上面の半導体チップ搭載領域に半導体チップ29が搭載される。

【0009】このようにして得られた半導体チップ実装体では、封止兼保護膜28が半導体チップ29の下面を保護(封止)する機能と引き回し線24、27を保護する機能とを兼ね備えることになるので、フィルム基板21が半導体チップ29の近傍で折り曲げられても、従来のような剥離現象が生じることがなく、したがって特に封止機能が損なわれることがなく、また封止兼保護膜28のみを形成すればよいので、製造工程数を少なくすることができる。

【0010】ここで、この半導体チップ実装体の寸法の一例について説明する。外部接続パッド22、25等の配線の厚さは8~18μm程度である。封止兼保護膜28のフィルム基板21上における厚さは、半導体チップ29のバンプ30、31の高さの1.5~2倍程度であ

る。封止兼保護膜28の外部接続パッド22、25等の配線上における厚さは、半導体チップ29のバンプ30、31の高さとほぼ同じである。したがって、バンプ30、31の高さが15μm程度であれば、封止兼保護膜28の外部接続パッド22、25等の配線上における厚さも15μm程度である。

【0011】なお、上記実施形態では、図1(C)に示すように、封止兼保護膜28の表面を平坦とした場合について説明したが、これに限定されるものではない。例えば、半導体チップ29の下面中央部に対応する部分における封止兼保護膜28の表面を適宜に盛り上げ、ポンディング時に半導体チップ29の下面で当該盛り上がり部を押し付けて平坦化するとともに、半導体チップ29の下面と封止兼保護膜28の表面との間に存在するエアーや押し出すようにしてもよい。このようにした場合には、半導体チップ29と封止兼保護膜28との間の密着力を上げることができる。

【0012】また、上記実施形態では、フィルム基板21の上面にラミネートされた銅箔等からなる導電膜をパターニングする場合について説明したが、これに限らず、例えばフィルム基板21の上面に接着剤層を介してラミネートされた銅箔等からなる導電膜をパターニングするようにしてもよい。さらに、上記実施形態では、半導体チップ29にバンプ30、31を設けた場合について説明したが、これに限らず、フィルム基板21の半導体チップ用接続パッド24、27上にバンプを設けるようにしてもよい。ただし、半導体チップ29の接続パッドがアルミニウムによって形成されている場合には、オーミックコンタクトを良好とするために、半導体チップ29のアルミニウムからなる接続パッド上に金属層(例えばTiW層とAu層の2層構造あるいはTi層とAu層の2層構造)を形成するようとする。

【0013】

【発明の効果】以上説明したように、この発明によれば、封止兼保護膜に封止機能と保護機能とを兼ね備えさせているので、従来のような剥離現象が生じることがなく、したがって特に封止機能が損なわれることがなく、また封止兼保護膜のみを形成すればよいので、製造工程数を少なくすることができる。

【図面の簡単な説明】

【図1】(A)~(D)はそれぞれこの発明の一実施形態における半導体チップ実装体の各製造工程の断面図。

【図2】従来の半導体チップ実装体の一例の断面図。

【符号の説明】

21 フィルム基板

22、25 外部接続パッド

23、26 半導体チップ用接続パッド

24、27 引き回し線

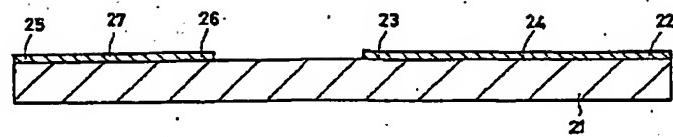
28 封止兼保護膜

29 半導体チップ

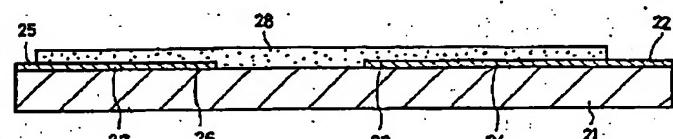
(4)

【図1】

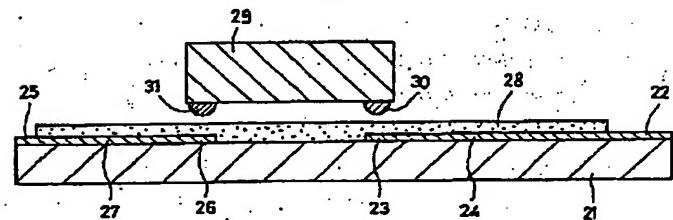
(A)



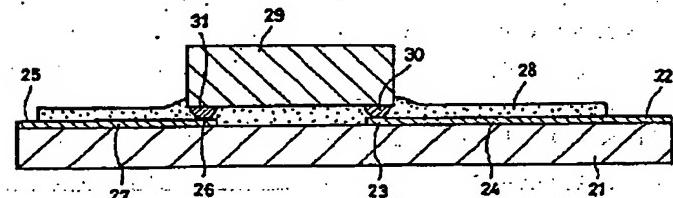
(B)



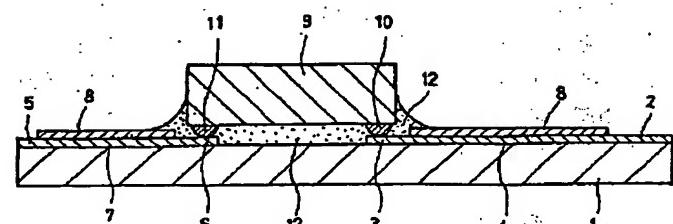
(C)



(D)



【図2】



**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**